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<u>L8</u>	L7 and 16	11	<u>L8</u>
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<u>L6</u>	L5 with (("L2" or level 2 or level two or secondary or second) adj3 cache)	79	<u>L6</u>
<u>L5</u>	buffer near6 (flush\$4 or cast\$3 or castout or purg\$4 or empt\$4 or remov\$4 or replac\$4 or eliminat\$4)	44160	<u>L5</u>
DB=	=USPT; PLUR=YES; OP=ADJ		
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<u>L3</u>	12 and (buffer or flush\$4 or cast\$3 or castout or purg\$4 or empt\$4 or remov\$4 or replac\$4 or eliminat\$4)	7	<u>L3</u>
<u>L2</u>	((store-through or writethrough or write-through or write adj through or store adj through) near4 cach\$4 and (read adj only or read-only) near4 (instruction adj2 cache) and (store-in or writeback or write-back or write adj back or store adj in) near4 cach\$4)	7	<u>L2</u>
DB=	=PGPB,USPT; PLUR=YES; OP=ADJ		

<u>L1</u>

(buffer near6 (flush\$4 or cast\$3 or castout or purg\$4 or empt\$4 or remov\$4 or replac\$4 or eliminat\$4) with (store-in or writeback or write-back or (write adj back) or (store adj in)) with cach\$4 and buffer near6 (flush\$4 or cast\$3 or castout or purg\$4 or empt\$4 or remov\$4 or replac\$4 or eliminat\$4) with ((lower level) or "L3" or (main memory)) and ((read-only or (read adj only)) near4 cach\$4))

0 <u>L1</u>

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L13 and ((input or output or first or second) near4 (queue or buffer))	0

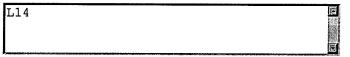
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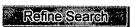
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<u>L13</u>	L12 and l11	2	<u>L13</u>
<u>L12</u>	L8 with 19	7	<u>L12</u>
<u>L11</u>	L10 with 19	53	<u>L11</u>
<u>L10</u>	((("L3" or level 3 or level three or main or lower) adj3 (cache or memory)))	21596	<u>L10</u>
<u>L9</u>	buffer near6 (flush\$4 or cast\$3 or castout or purg\$4 or empt\$4 or remov\$4 or replac\$4 or eliminat\$4 or writeback)	8217	<u>L9</u>
<u>L8</u>	(store-in or writeback or write-back or write adj back or store adj in) near4 cach\$4	466	<u>L8</u>
DB=P	PGPB,USPT; PLUR=YES; OP=ADJ		
<u>L7</u>	L6 and ((input or output or first or second) near4 (queue or buffer))	9	<u>L7</u>
<u>L6</u>	L5 and 14	11	<u>L6</u>
<u>L5</u>	L2 with 11	126	<u>L5</u>

<u>L4</u>	L3 with 12	213	<u>L4</u>
<u>L3</u>	((("L3" or level 3 or level three or main or lower) adj3 (cache or memory)))	46319	<u>L3</u>
<u>L2</u>	buffer near6 (flush\$4 or cast\$3 or castout or purg\$4 or empt\$4 or remov\$4 or replac\$4 or eliminat\$4 or writeback)	44271	<u>L2</u>
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Afzal Malik, Bill Moyer, Roger Zhou

October 2002 Proceedings of the international conference on Compilers, architecture, as

Full text available: pdf(122.19 KB)

Additional Information: full citation, abstract, referen

Next generation portable devices are placing stringent requirements on overall system power and wire less internet access are just some of the features being incorporated in these handheld elections for high performance and cost sensitive portable products as well as for high end embedded contri M¿CORE M2 and M310 fami ...

Keywords: cache control, cache management, copyback, programmable, push buffer, write buffe

2 An effective write policy for software coherence schemes

Y.-C. Chen, A. V. Veidenbaum

December 1992 Proceedings of the 1992 ACM/IEEE conference on Supercomputing

Full text available: pdf(1.14 MB)

Additional Information: full citation, references, index terms

Cache write policies and performance

Norman P. Jouppi

May 1993

ACM SIGARCH Computer Architecture News, Proceedings of the 20th ann

Volume 21 Issue 2

Full text available: pdf(1.14 MB)

Additional Information: full citation, abstract, referen

This paper investigates issues involving writes and caches. First, tradeoffs on writes that miss in the block is fetched on a write miss, whether the missed cache block is allocated in the cache, and wh considered. Depending on the combination of these polices chosen, the entire cache miss rate can no- ...

Coherent network interfaces for fine-grain communication

Shubhendu S. Mukherjee, Babak Falsafi, Mark D. Hill, David A. Wood

May 1996 ACM SIGARCH Computer Architecture News, Proceedings of the 23rd ann

Volume 24 Issue 2

Full text available: pdf(1.72 MB)

Additional Information: full citation, abstract, referen



Historically, processor accesses to memory-mapped device registers have been marked uncachabl cache coherence, however, makes it possible for processors and devices to interact with cachable, performance by facilitating burst transfers of whole cache blocks and reducing control overheads (interfaces (NIs) that u ...

Silent stores for free

Kevin M. Lepak, Mikko H. Lipasti

December 2000 Proceedings of the 33rd annual ACM/IEEE international symposium on Micro

Full text available: pdf(521.75 KB) ps(1.97 MB)

Additional Information: full citation, references, citings, index

Publisher Site

An evaluation of memory consistency models for shared-memory systems with ILP processor Vijay S. Pai, Parthasarathy Ranganathan, Sarita V. Adve, Tracy Harton

September 1996 Proceedings of the seventh international conference on Architectural supp Volume 31, 30 Issue 9, 5

Full text available: pdf(1.64 MB)

Additional Information: full citation, abstract, referen

Relaxed consistency models have been shown to significantly outperform sequential consistency for However, current microprocessors aggressively exploit instruction-level parallelism (ILP) using me blocking reads. Researchers have conjectured that two techniques, hardware-controlled non-binding equalize the hardware pe ...

7 A coherent distributed file cache with directory write-behind

Timothy Mann, Andrew Birrell, Andy Hisgen, Charles Jerian, Garret Swart ACM Transactions on Computer Systems (TOCS), Volume 12 Issue 2

May 1994 Full text available: 1 pdf(3.21 MB)

Additional Information: full citation, abstract, referen

Extensive caching is a key feature of the Echo distributed file system. Echo client machines mainta write-behind (delayed write-back) of all cached information. Echo specifies ordering constraints on consistent data structures in the file system even when crashes or network faults prevent some will

Keywords: coherence, file caching, write-behind

Cache Memories

Alan Jav Smith

September 1982 ACM Computing Surveys (CSUR), Volume 14 Issue 3

Full text available: pdf(4.61 MB)

Additional Information: full citation, references, citings, ind

Translation lookaside buffer consistency: a software approach

D. L. Black, R. F. Rashid, D. B. Golub, C. R. Hill

April 1989

ACM SIGARCH Computer Architecture News, Proceedings of the third inte programming languages and operating systems, Volume 17 Issue 2

Full text available: pdf(1.38 MB)

Additional Information: full citation, abstract, referen

We discuss the translation lookaside buffer (TLB) consistency problem for multiprocessors, and int consistency in software. This algorithm has been implemented on several multiprocessors, and is i basic costs of the algorithm and show that it has minimal impact on application performance. As a to multiprocessor ...

10 Implementing a cache for a high-performance GaAs microprocessor

h cf c g e

O. A. Olukotun, T. N. Mudge, R. B. Brown

April 1991 ACM SIGARCH Computer Architecture News, Proceedings of the 18th ann

Volume 19 Issue 3

Full text available: pdf(1.12 MB)

Additional Information: full citation, references, citin

11 The directory-based cache coherence protocol for the DASH multiprocessor

Daniel Lenoski, James Laudon, Kourosh Gharachorloo, Anoop Gupta, John Hennessy

May 1990 ACM SIGARCH Computer Architecture News, Proceedings of the 17th ann

Volume 18 Issue 3

Full text available: pdf(1.74 MB)

Additional Information: full citation, abstract, referer

DASH is a scalable shared-memory multiprocessor currently being developed at Stanford's Compu processing nodes, each with a portion of the shared-memory, connected to a scalable interconnect based cache coherence protocol. Unlike traditional snoopy coherence protocols, the DASH protocol messages sent between th ...

12 Performance of database workloads on shared-memory systems with out-of-order processor

Parthasarathy Ranganathan, Kourosh Gharachorloo, Sarita V. Adve, Luiz André Barroso

October 1998 Proceedings of the eighth international conference on Architectural support

Volume 33 , 32 Issue 11 , 5

Full text available: pdf(1.62 MB)

Additional Information: full citation, abstract, referen

Database applications such as online transaction processing (OLTP) and decision support systems market for multiprocessor servers. However, most current system designs have been optimized to radically different behavior of database workloads (especially OLTP), it is important to re-evaluate of applicatio ...

13 Memory system performance of programs with intensive heap allocation

Amer Diwan, David Tarditi, Eliot Moss

August 1995 ACM Transactions on Computer Systems (TOCS), Volume 13 Issue 3

Full text available: pdf(2.10 MB)

Additional Information: full citation, abstract, referen

Heap allocation with copying garbage collection is a general storage management technique for pr performance. To investigate this, we conducted an in-depth study of the memory system performance machines. We studied the performance of mostly functional Standard ML programs which made he heap allocation poorly. Howeve ...

Keywords: automatic storage reclamation, copying garbage collection, garbage collection, general placement, write through, write-back, write-buffer, write-miss policy, write-policy

14 A scalable approach to thread-level speculation

J. Greggory Steffan, Christopher B. Colohan, Antonia Zhai, Todd C. Mowry

May 2000 ACM SIGARCH Computer Architecture News, Proceedings of the 27th ann

Volume 28 Issue 2

Full text available: pdf(186.97 KB)

Additional Information: full citation, abstract, referen

While architects understand how to build cost-effective parallel machines across a wide spectrum (servers), the real challenge is how to easily create parallel software to effectively exploit all of this overcoming this problem is Thread-Level Speculation (TLS), which enables the compiler to optimis

15 Compiler and hardware support for cache coherence in large-scale multiprocessors: design Lynn Choi, Pen-Chung Yew

May 1996 ACM SIGARCH Computer Architecture News, Proceedings of the 23rd ann Volume 24 Issue 2

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Full text available: pdf(1.48 MB)

Additional Information: full citation, abstract, referen

In this paper, we study a hardware-supported, compiler directed (HSCD) cache coherence scheme off-the-shelf microprocessors, such as the Cray T3D. It can be adapted to various cache organizat architectures. Several system related issues, including critical sections, inter-thread communicatio required hardware sup ...

¹⁶ Architecture and design of AlphaServer GS320

Kourosh Gharachorloo, Madhu Sharma, Simon Steely, Stephen Van Doren

November 2000 Proceedings of the ninth international conference on Architectural suppor

28 , 34 Issue 5 , 5

Full text available: pdf(413.91 KB)

Additional Information: full citation, abstract, referen

This paper describes the architecture and implementation of the AlphaServer GS320, a cache-cohe Compaq. The AlphaServer GS320 architecture is specifically targeted at medium-scale multiproces four Alpha 21264 processors, up to 32GB of coherent memory, and an aggressive IO subsystem. of 32 processors. While s ...

17 Architecture and design of AlphaServer GS320

Kourosh Gharachorloo, Madhu Sharma, Simon Steely, Stephen Van Doren

November 2000 ACM SIGPLAN Notices, Volume 35 Issue 11

Full text available: pdf(1.67 MB)

Additional Information: full citation, abstract, referer

This paper describes the architecture and implementation of the AlphaServer GS320, a cache-cohe Compaq. The AlphaServer GS320 architecture is specifically targeted at medium-scale multiproces four Alpha 21264 processors, up to 32GB of coherent memory, and an aggressive IO subsystem. of 32 processors. While s ...

18 Data speculation support for a chip multiprocessor

Lance Hammond, Mark Willey, Kunle Olukotun

October 1998 Proceedings of the eighth international conference on Architectural suppo

Volume 32, 33 Issue 5, 11

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Additional Information: full citation, abstract, referen

Thread-level speculation is a technique that enables parallel execution of sequential applications o implementation of the support for threadlevel speculation on the Hydra chip multiprocessor (CMP) handlers and modifications to the shared secondary cache memory system of the CMP This suppor results show that the s ...

19 Cache behavior of combinator graph reduction

Philip J. Koopman, Peter Lee, Daniel P. Siewiorek

April 1992 ACM Transactions on Programming Languages and Systems (TOPLAS), Vol

Full text available: pdf(2.18 MB)

Additional Information: full citation, abstract, referen

The results of cache-simulation experiments with an abstract machine for reducing combinator grareduction rates that, for similar kinds of combinator graphs on similar kinds of hardware, compare TIGRE maps easily and efficiently onto standard computer architectures, particularly those that all indication th ...

Keywords: abstract machine, combinators, graph reduction, self-modifying code

²⁰ Improving I/O performance with a conditional store buffer

Lambert Schaelicke, Al Davis

November 1998 Proceedings of the 31st annual ACM/IEEE international symposium on Micro

Full text available: pdf(2.53 MB)

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